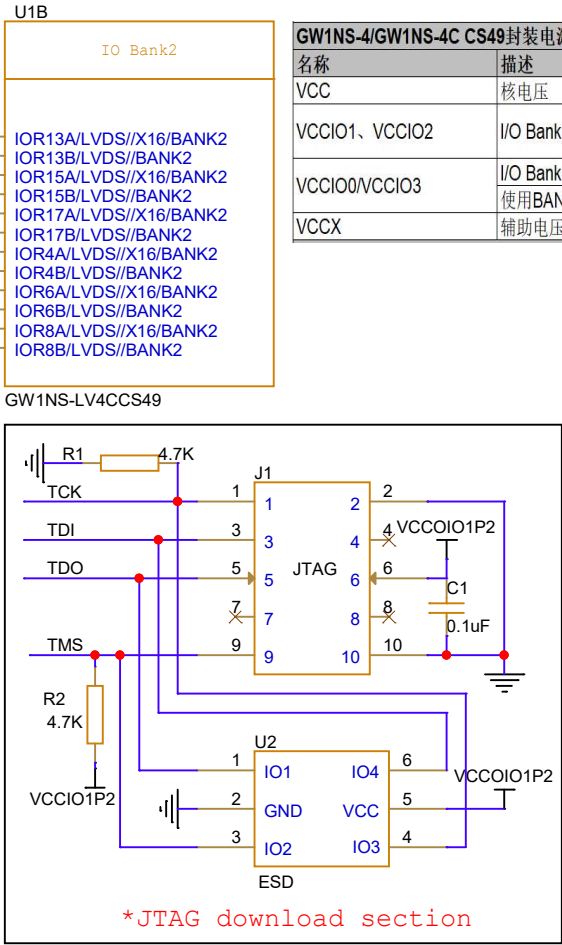
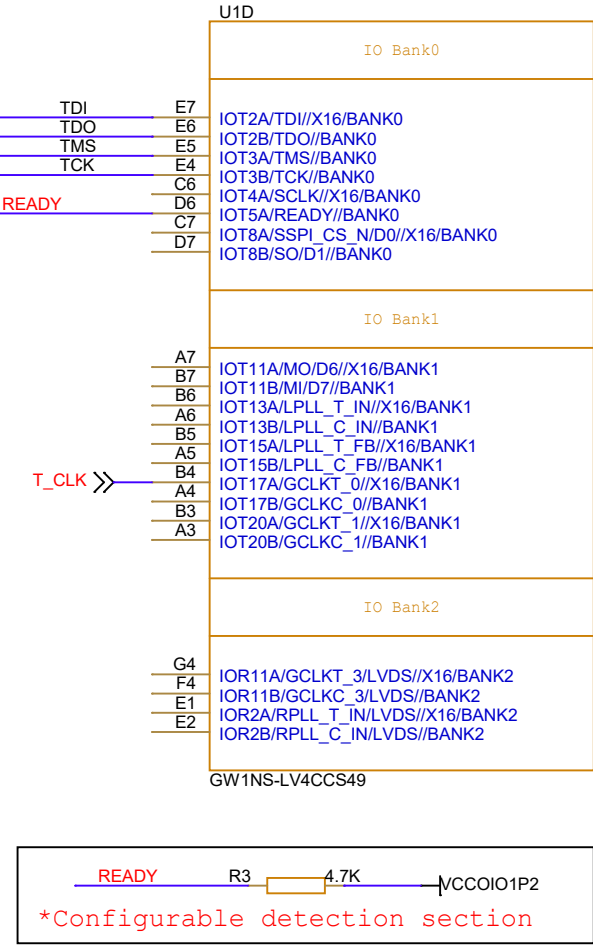
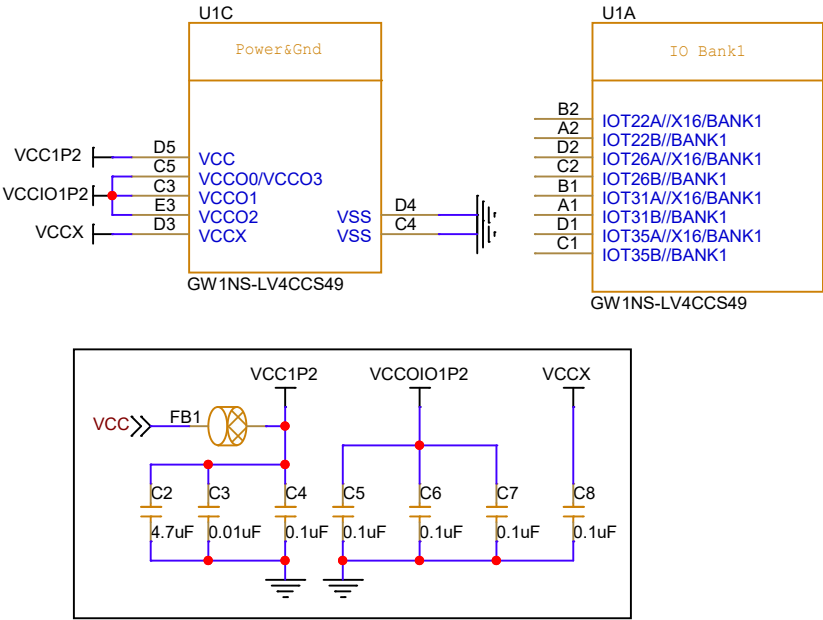


GW1NS-LV4CCS49

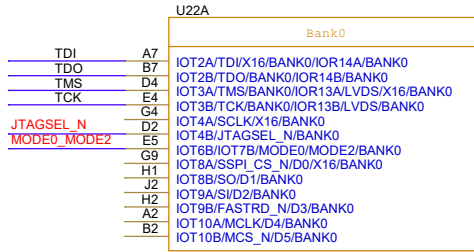


GW1NS-4/GW1NS-4C CS49封装电源供电要求			
名称	描述	最小值	最大值
VCC	核电压	1.14V	1.26V
VCCIO1、VCCIO2	I/O Bank电压 使用BANK1的MIPI输入时，VCCIO1需供1.2V 使用BANK2的MIPI输出时，VCCIO2需供1.2V	1.14V	3.6V
VCCIO0/VCCIO3	I/O Bank电压，VCCIO0/VCCIO3内部连接在一起 使用BANK0的MIPI输入时，VCCIO0需供1.2V	1.14V	3.6V
VCCX	辅助电压	1.71V	3.6V

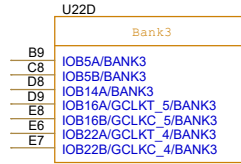


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.VCCX should be greater than or equal to VCCIO.

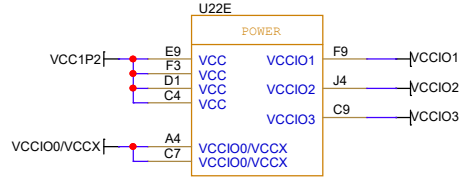
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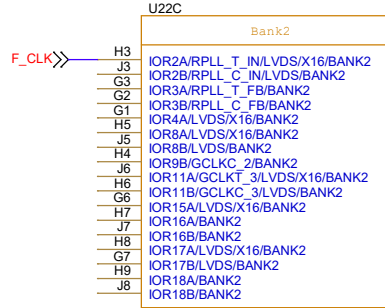
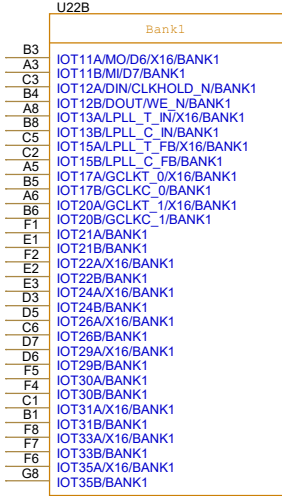
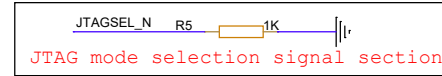
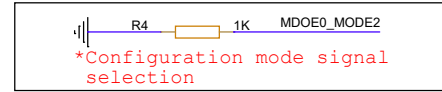
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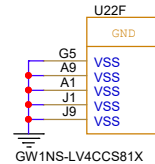
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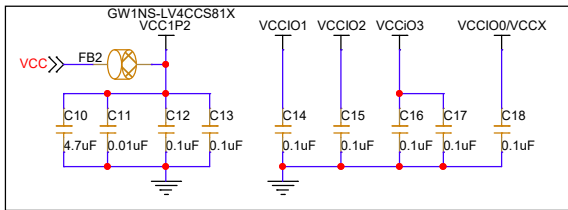
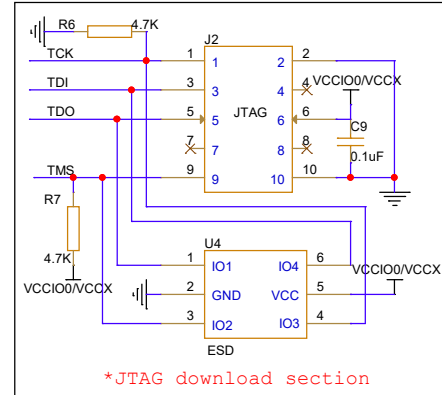
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GW1NS-LV4CCS81X



GW1NS-LV4CCS81X



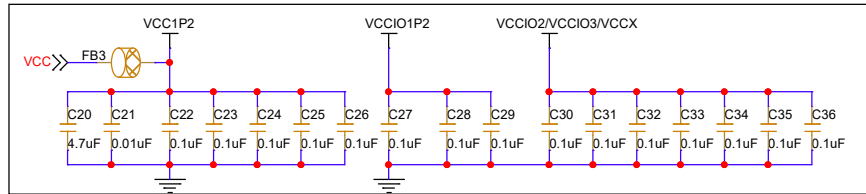
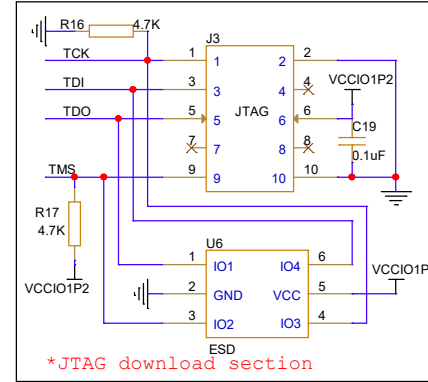
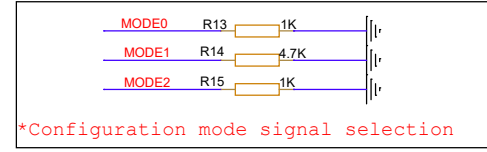
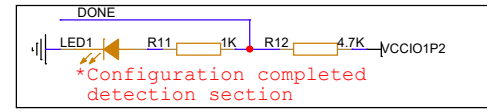
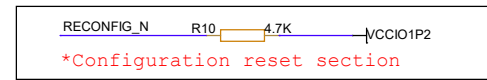
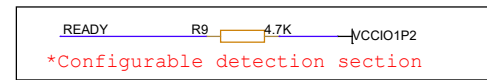
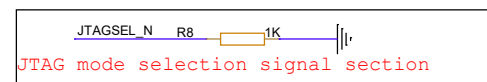
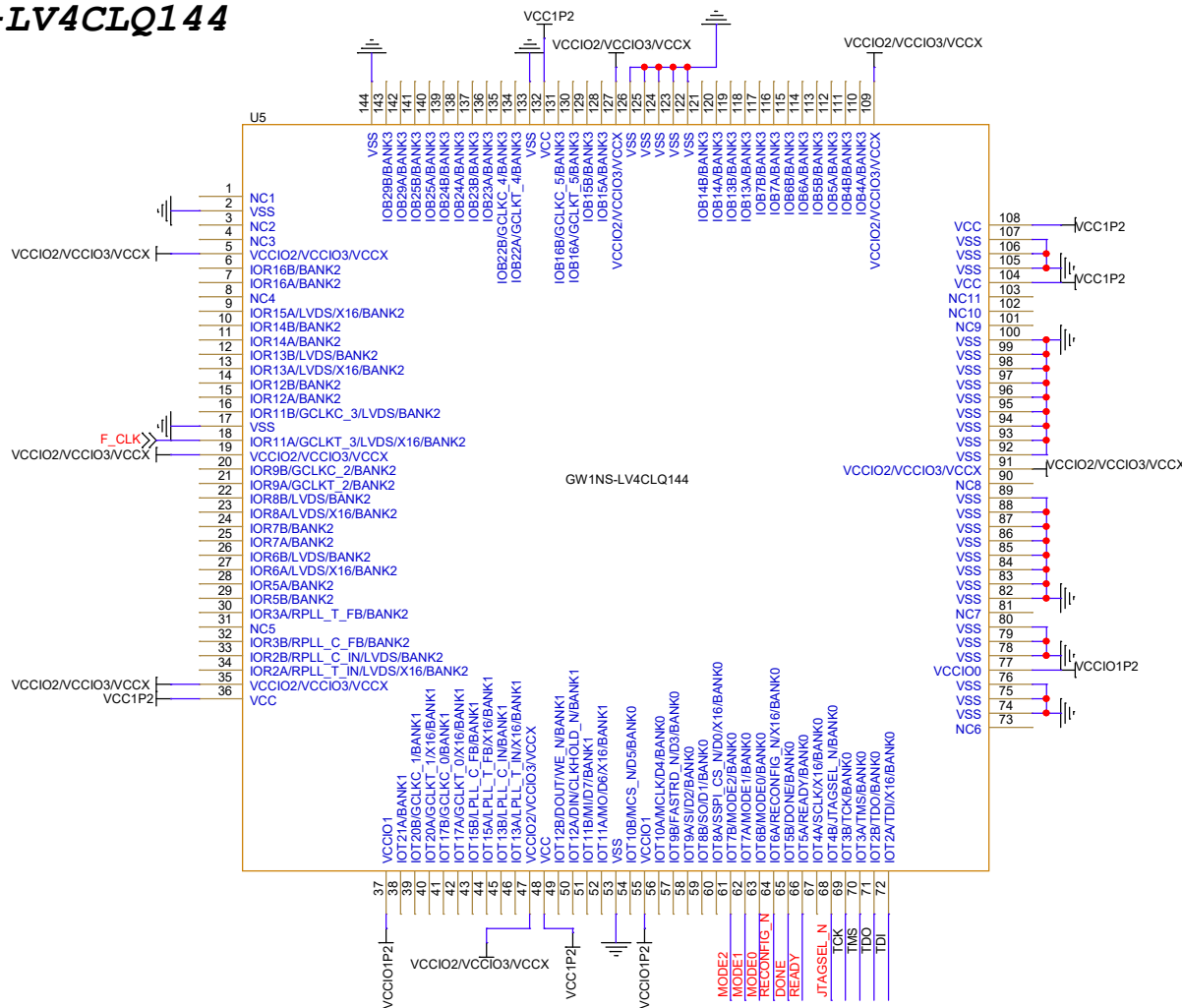
Recommended Operating Conditions of CS81X Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V
VCCIO0/VCCX	I/O Bank voltage VCCIO0 and auxiliary voltage VCCX are internally connected.	1.71V	3.6V

Notes:

- 1.F CLK signal is an external input clock signal.
- 2.It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCCX should be greater than or equal to VCCIO.
- 5.For background upgrade of CS81X package, VCCIO0 and VCCIO2 must be supplied with the same voltage.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1NS-LV4CCS81X	2.6
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GW1NS-LV4CLQ144

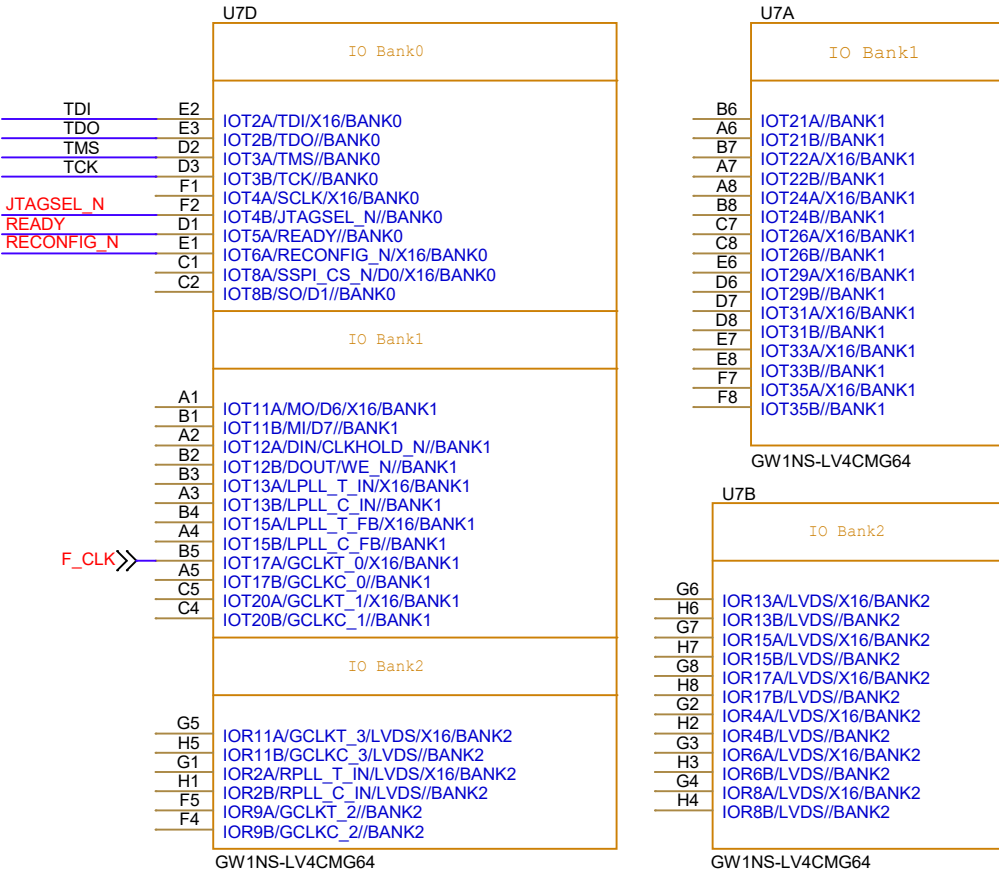


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.VCCX should be greater than or equal to VCCIO.

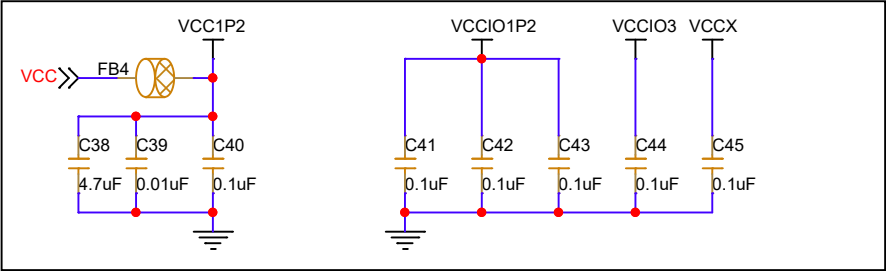
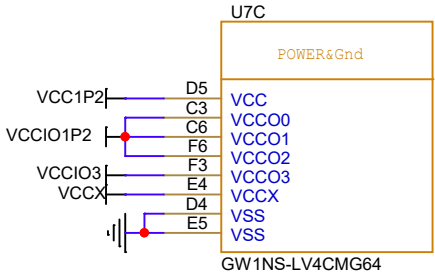
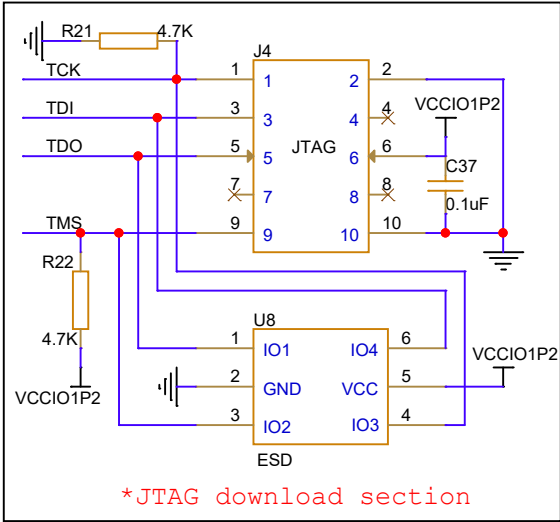
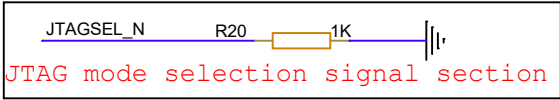
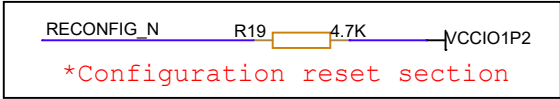
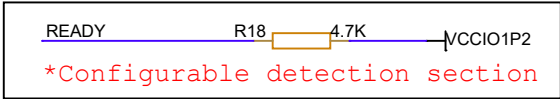
Recommended Operating Conditions of LQ144 Package in GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage.	1.14V	3.6V
VCCIO2/VCCIO3/VCCX	I/O Bank voltage VCCIO2/VCCIO3 and auxiliary voltage VCCX are internally connected.	1.71V	3.6V

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1NS-LV4CLQ144	2.5
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	Sheet	3 of 10

GW1NS-LV4CMG64



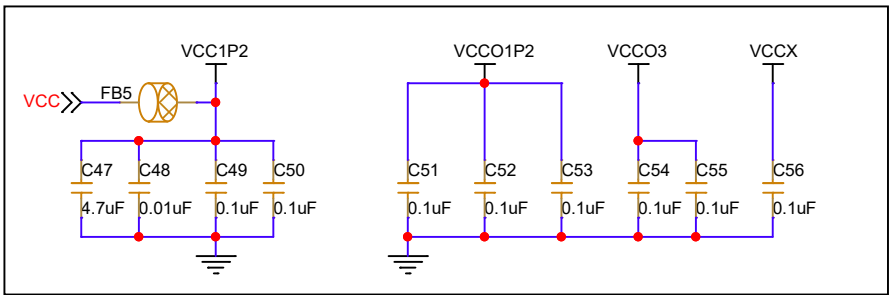
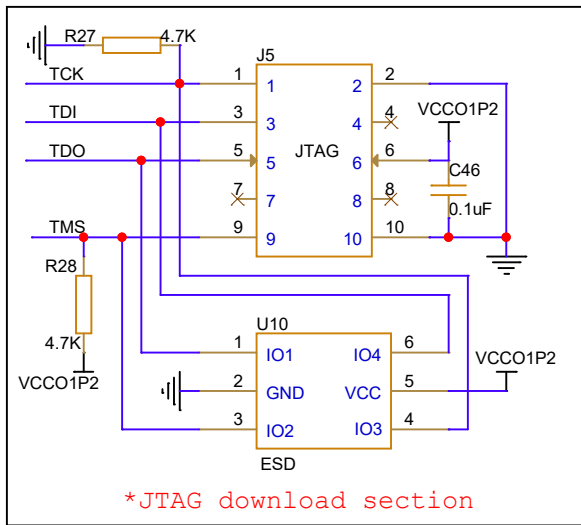
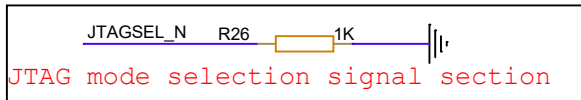
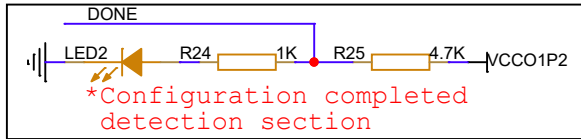
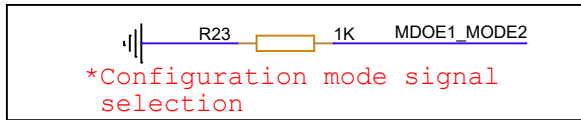
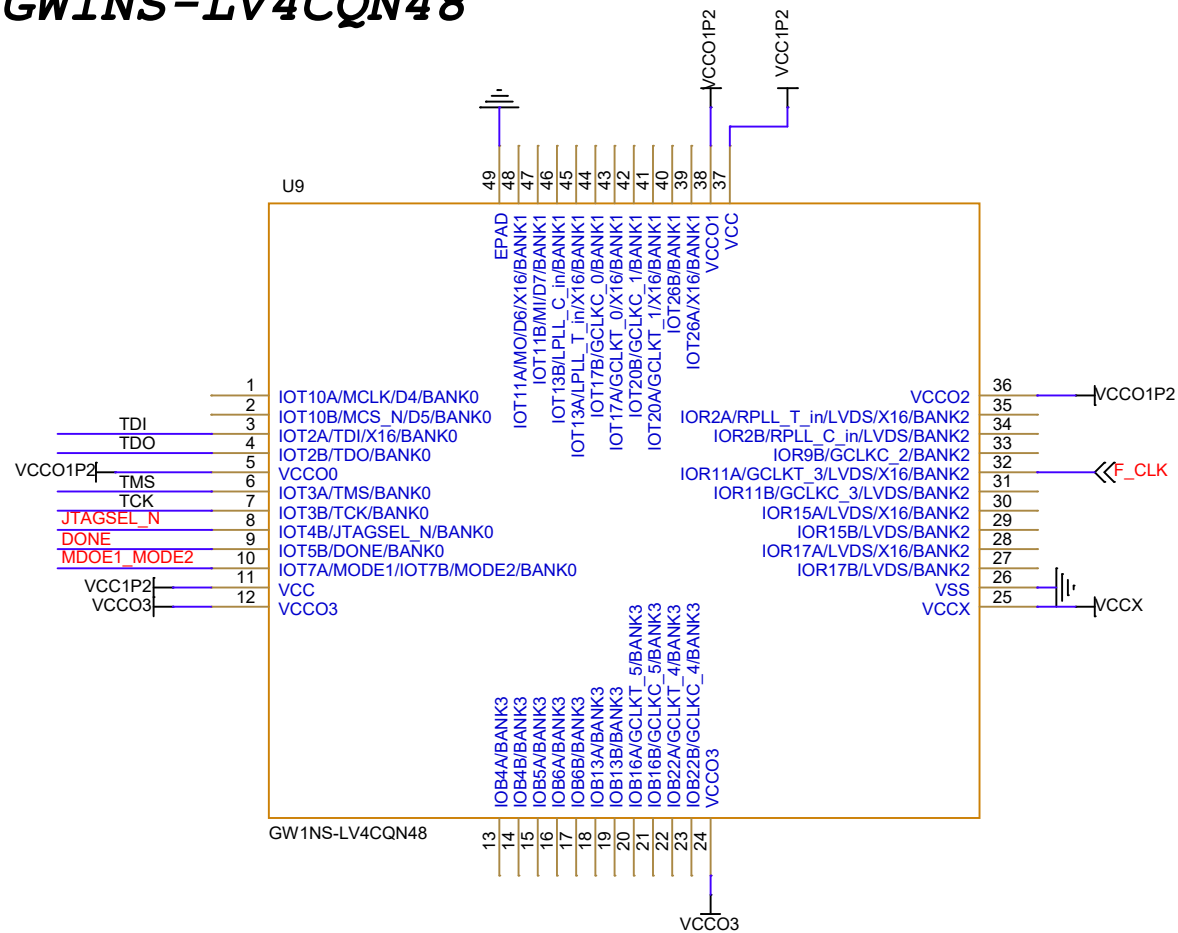
Recommended Operating Conditions of MG64 Package in GW1NS-4/GW1NS-4C				
Name	Description		Min.	Max.
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage		1.71V	3.6V



- Notes:
- F_CLK signal is an external input clock signal.
 - It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - It is recommended that add an ESD protection chip to the JTAG download circuit
 - VCCX should be greater than or equal to VCCIO.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NS-LV4CMG64	2.5
Date: Friday, June 27, 2025		
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GW1NS-LV4CQN48

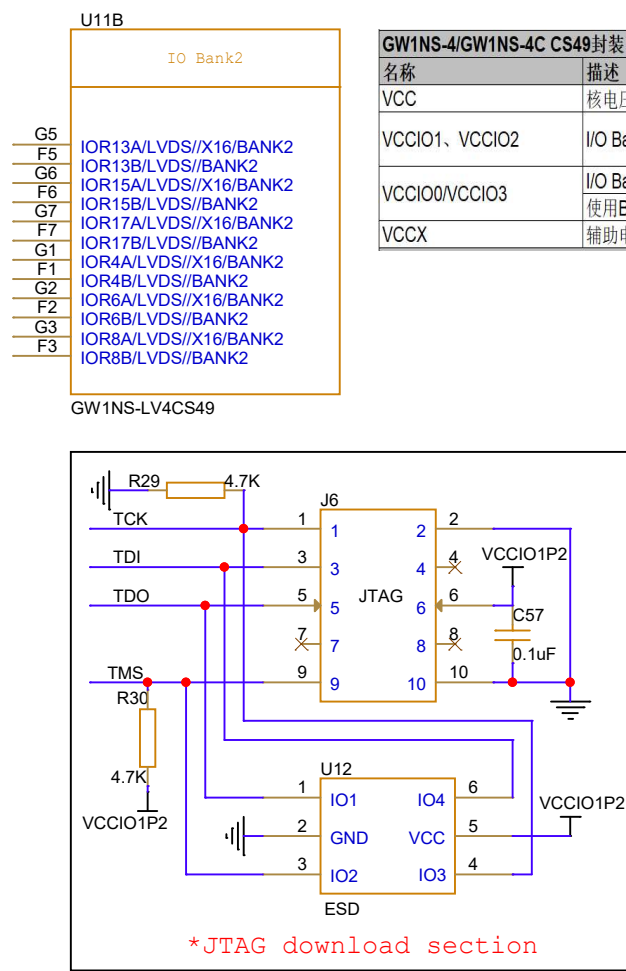
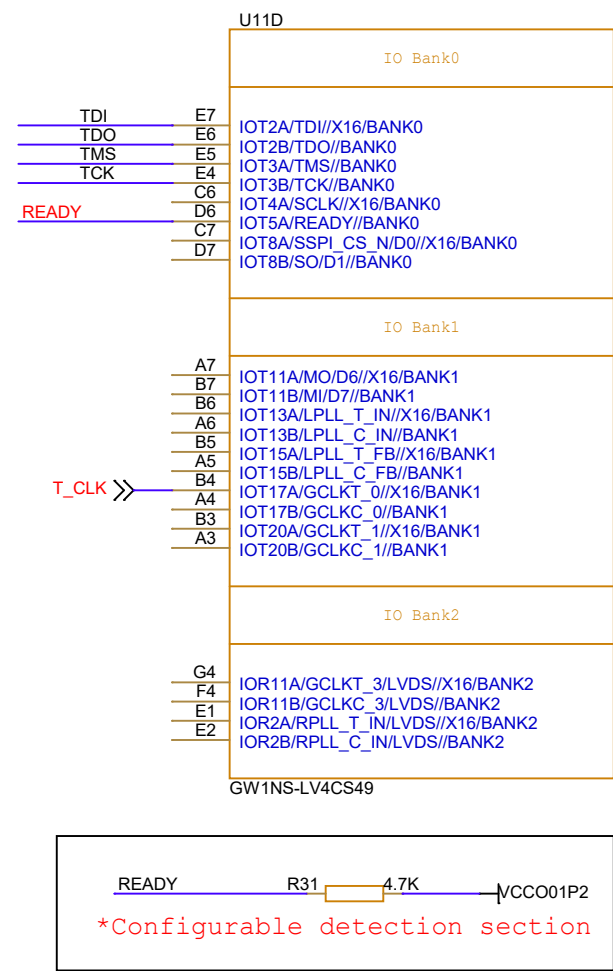


Recommended Operating Conditions of QN48 Package in GW1NS-4/GW1NS-4C				
Name	Description		Min.	Max.
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage		1.71V	3.6V
Note!				
It is highly recommended that the EPAD connect to GND, but not a requirement.				

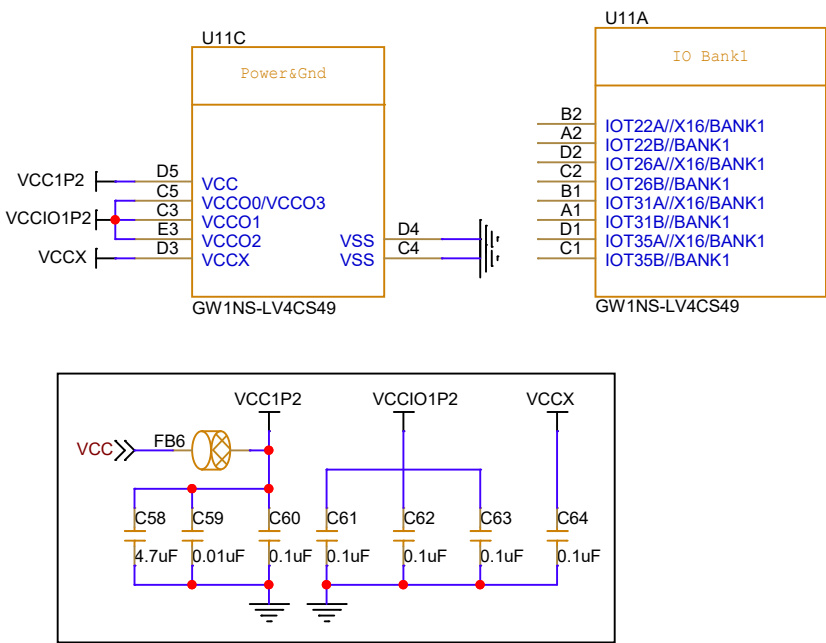
- Notes:
- F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - It is recommended that add an ESD protection chip to the JTAG download circuit.
 - VCCX should be greater than or equal to VCCIO.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NS-LV4CQN48	2.5
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GW1NS-LV4CS49

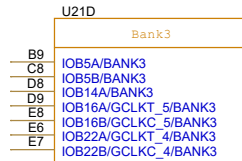
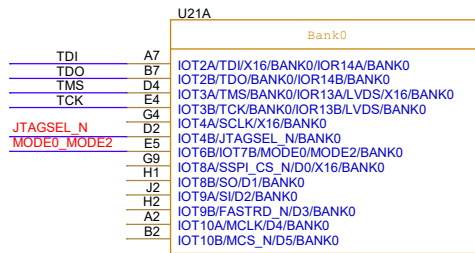


GW1NS-4/GW1NS-4C CS49封装电源供电要求			
名称	描述	最小值	最大值
VCC	核电压	1.14V	1.26V
VCCIO1、VCCIO2	I/O Bank电压 使用BANK1的MIPI输入时，VCCIO1需供1.2V 使用BANK2的MIPI输出时，VCCIO2需供1.2V	1.14V	3.6V
VCCIO0/VCCIO3	I/O Bank电压，VCCIO0/VCCIO3内部连接在一起 使用BANK0的MIPI输入时，VCCIO0需供1.2V	1.14V	3.6V
VCCX	辅助电压	1.71V	3.6V

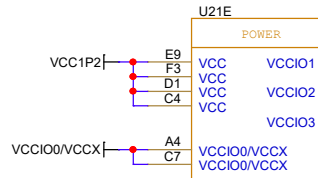


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.VCCX should be greater than or equal to VCCIO.

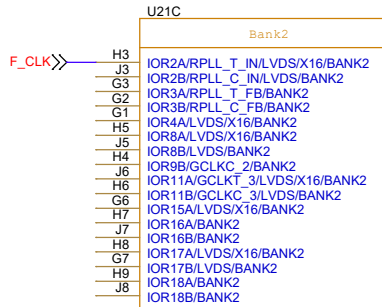
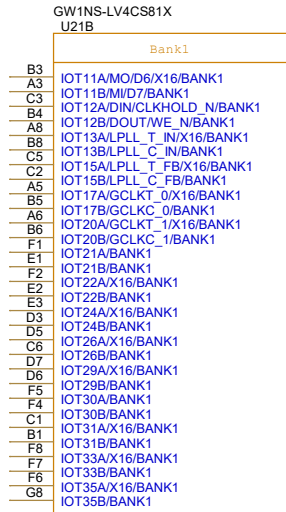
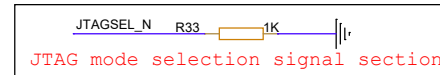
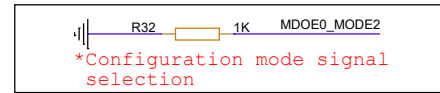
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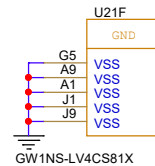
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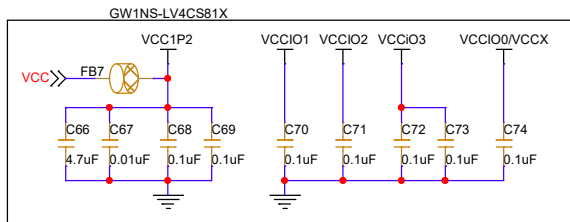
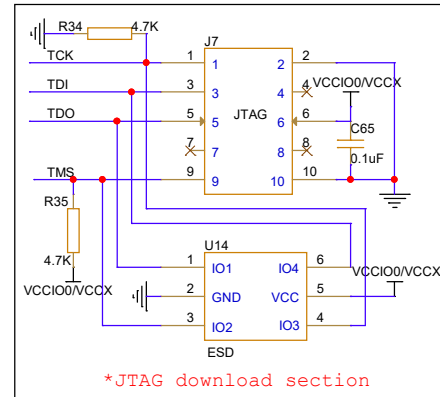
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GW1NS-LV4CS81X



GW1NS-LV4CS81X



Recommended Operating Conditions of CS81X Package in GW1NS-4/GW1NS-4C

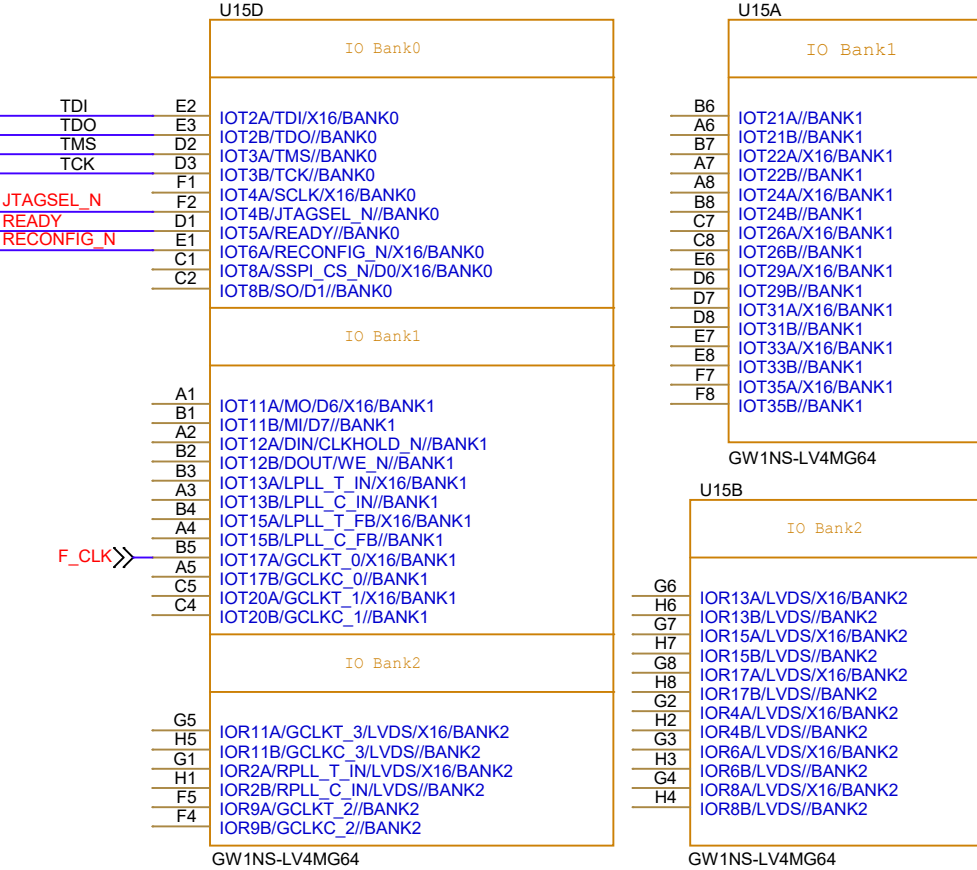
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V
VCCIO0/VCCX	I/O Bank voltage VCCIO0 and auxiliary voltage VCCX are internally connected.	1.71V	3.6V

Notes:

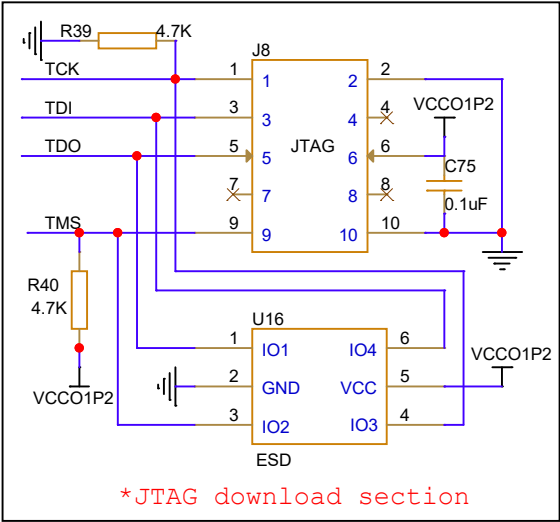
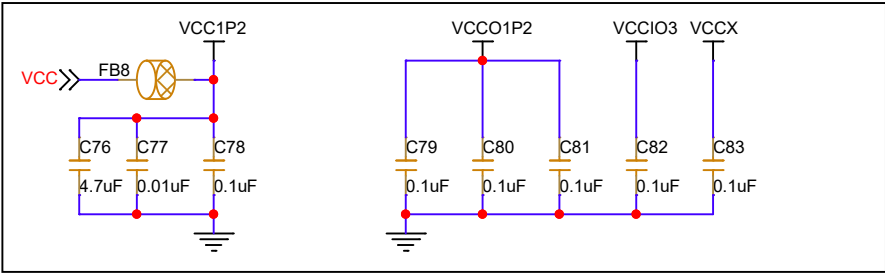
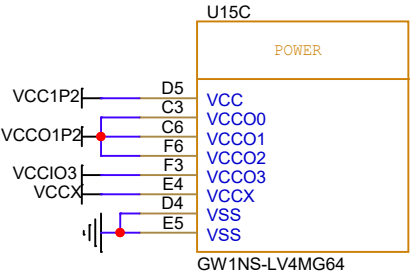
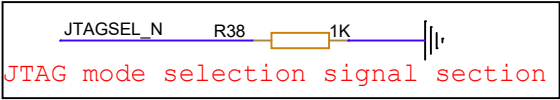
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 3.VCCX should be greater than or equal to VCCIO.
- 4.For background upgrade of CS81X package, VCCIO0 and VCCIO2 must be supplied with the same voltage.

Title		
GOWIN Minimum System Diagram		
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GW1NS-LV4MG64



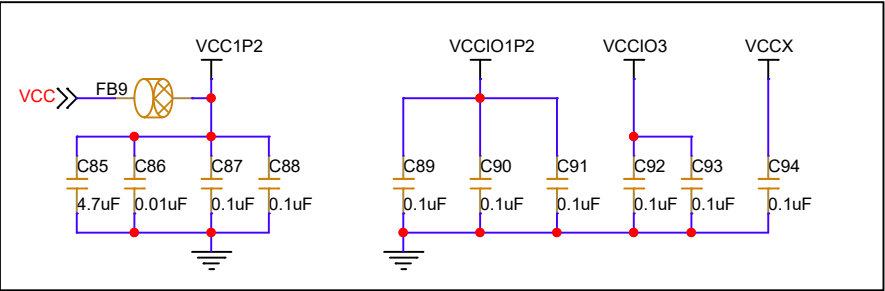
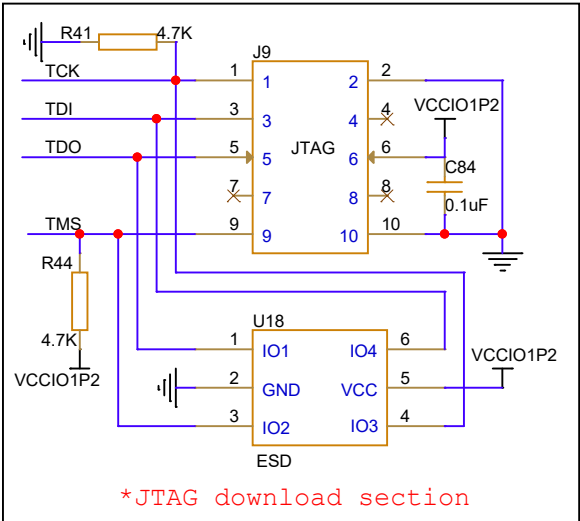
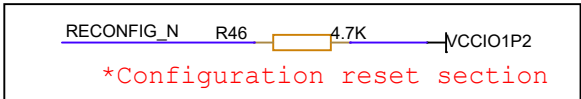
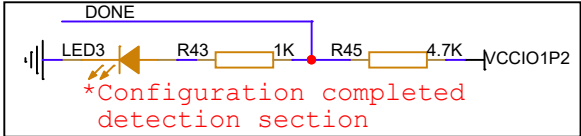
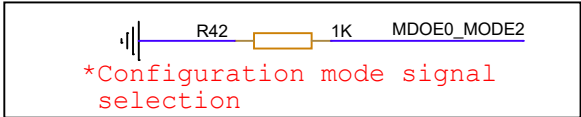
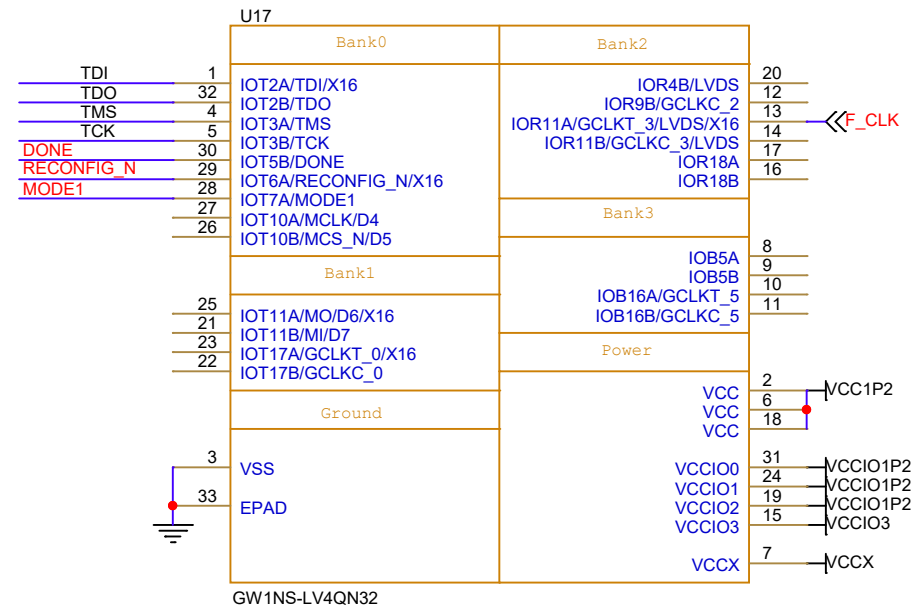
Recommended Operating Conditions of MG64 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V



- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.VCCX should be greater than or equal to VCCIO.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NS-LV4MG64	2.5
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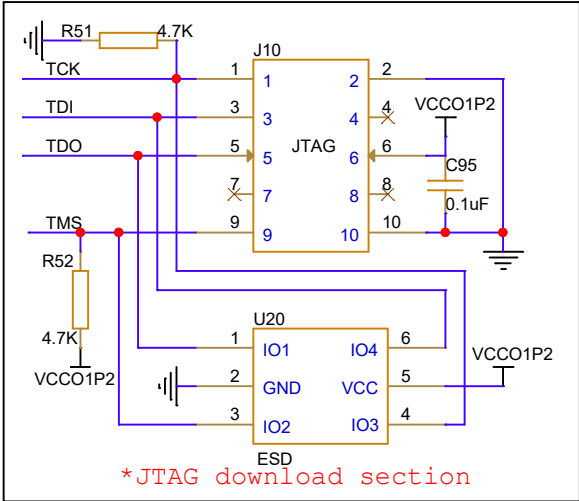
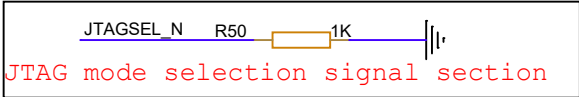
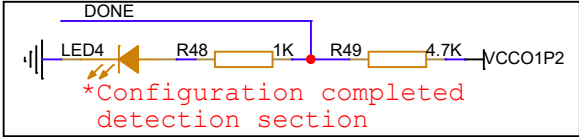
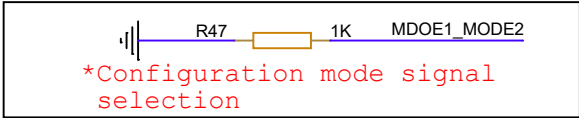
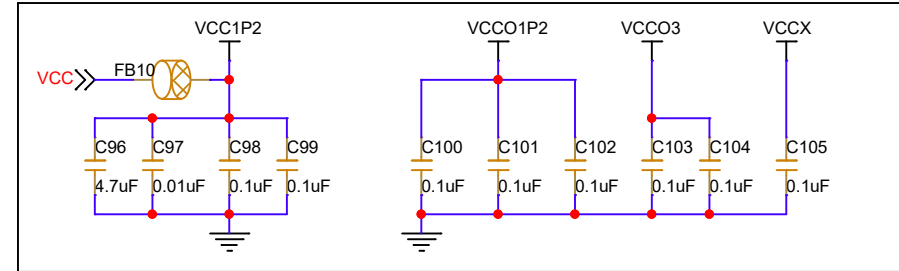
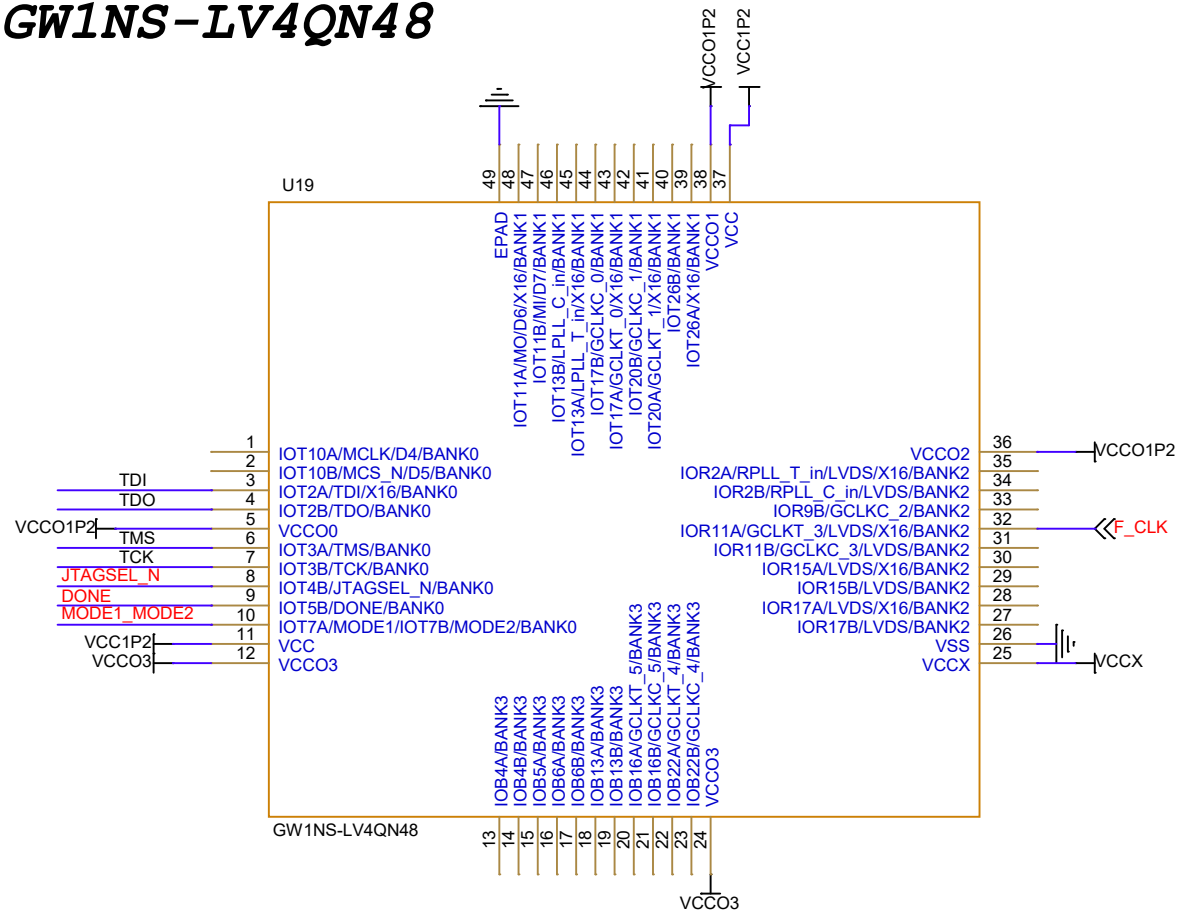
GW1NS-LV4QN32



Recommended Operating Conditions of QN32 Package in GW1NS-4				
Name	Description		Min.	Max.
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage		1.71V	3.6V
Note !				
It is highly recommended that the EPAD connect to GND, but not a requirement.				

- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.VCCX should be greater than or equal to VCCIO.

GW1NS-LV4QN48



Recommended Operating Conditions of QN48 Package in GW1NS-4/GW1NS-4C				
Name	Description		Min.	Max.
VCC	Core voltage		1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage		1.71V	3.6V
Note! It is highly recommended that the EPAD connect to GND, but not a requirement.				

- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.VCCX should be greater than or equal to VCCIO.

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GOWIN Minimum System Diagram			
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